CS/B.TECH/CSE(O)/ODD/SEM-5/CS-502/2019-20



MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code: CS-502

PUID: 05013(To be mentioned in the main answer script)

MICROPROCESSORS AND MICRO-CONTROLLERS

Time Allotted: 3 Hours

Full Marks: 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP - A

(Multiple Choice Type Questions)

- 1. Choose the correct alternatives for any ten of the following: $10 \times 1 = 10$
 - i) The frequency of CLOCK OUT signal of 8085 microprocessor is
 - a) 6 MHz

b) 3 MHz

c) 6kHz

- d) 2 MHz.
- ii) The interrupt pin available in the 8085A microprocessor chip is
 - a) ALE

b) HOLD

c) INTR

d) SOD.

**-5201/5(O)

[Turn over

iii)	When the RET instruction at the end of sub-routing						
	exe	cuted					
	a) the information where the stack is initialized is						
		transferred to the s	tack	pointer			
	b)	the memory addres	s of	the RET instruction is			
		transferred to the P	C ·				
	c)	two data bytes stor	ed in	n the top two locations			
		of the stack are tran	nsfer	red to the PC			
	d)	two data bytes stor	ed ir	the top two locations			
		of the stack are trar	sfer	red to the SP.			
iv)	v) A single instruction to clear the lower four bits						
*	the	accumulator in 8085	mic	roprocessor is			
	a)	XRI OFH .	b)	ANI FOH			
	c)	ANI OFH	d)	XRI FOH.			
v)	Mac	hine cycles in "CALL	" ins	truction are			
	a)	6	b)	5			
	c)	4	d)	3.			
vi)	Address lines required for 32 k-byte memory chip						
	are			comp			
	a)	13	b)	14			
	c)	15	d)	16.			
vii)	The call location for TRAP interrupt is						
	a)	0000Н	b)	0020H			
	c)	0024H	d)	0034Н.			
* -520	1/5(0						

viii	sta	What will be the content of the accumulator and status of CY flag after RLC operation, if the content of the accumulator is BC H and CY is 0?					
	a)		b)				
	c)	5E H, 0	d)	5D H, 0.			
ix)	Šele	Select the invalid instruction:					
	a)	MOV M, A	b)	ADI 67			
	c)	LDAX B	d)	STAX H.			
x)	Wha	What is the function of the instruction DAD B?					
	a)	It adds B register and	d C	register			
	b)	It adds B register to	D re	gister			
	c)	It adds B-C register p	pair	and H-L register pair			
	d)	It adds B-C register I	pair.				
xi)	The	The instruction, MOV AX, [2500H] is an example of					
	a)	immediate addressin	g mo	ode			
	b)	direct addressing mo	de				
	c)	indirect addressing n	node				
	d)	register addressing m	node	•			
xii)	EU	is used for					
	a)	encoding	b)	fetching			
	c)	decoding	d)	both (a) and (b).			
				* *			

GROUP - B

(Short Answer Type Questions)

Answer any three of the following. $3 \times 5 = 15$

2. If the system clock is 2MHz, find the time to execute the given instruction code:

 $MVIA, 5A_H$

MHI B, A7_H

ADD B

INR A

XRA A

HLT

3. In memory mapped I/O, how does microprocessor differentiate between an I/O and Memory? Can Memory and I/O have the same address? Compare Memory mapped I/O and Peripheral mapped I/O.

2 + 1 + 2

- 4. Discuss the functions of following instructions of 8085 microprocessor : 5×1 LHLD 8050_H, RLC, LDAX B, DAD D, STA 2000_H
- Write an assembly language program in 8085 to count the number of 1s and number of 0s in a data byte and store the counts in two different memory locations.
- Describe the different addressing modes of 8086 microprocessor.

GROUP - C

(Long Answer Type Questions)

Answer any three of the following. $3 \times 15 = 45$

7. a) Specify the content of Accumulator and Flag when the following instructions are executed. 2 + 2

MVI A, 01_H

MVI B, 02_H

ADD B

XRA A

HLT

- b) Differentiate between absolute memory address decoding and partial memory address decoding. 2
- c) Explain the memory address range of 1K-byte R/W memory by using partial decoding for 8085 microprocessor.
- d) What are the functions of RESET, INTR, HOLD, READY, HLDA pins of 8085 microprocessor?
- 8. a) Explain the instruction execution cycle of IN 01_H by using timing diagram.
 - b) Why is demultiplexing address/data bus needed?

 How 8085 microprocessor demultiplexes address/data bus?

 2 + 2

	c)	If size of the memory chip is 2048 × 8 bits, how
		many chips are required to make up 16K-byte memory?
	d)	What is subroutine? Briefly discuss the sequence of events that takes place while executing CALL instruction. 1 + 3
9.	a)	What are the different interrupts in 8085? Give their locations? Distinguish between maskable and non-maskable interrupts. $2+2+2$
	b)	Write the accumulator bit pattern for SIM and RIM instrutions.
	c)	Write the program for enable the RST-7.5, RST-6.5 and disable RST-5.5.
	d)	Explain in brief the different transfer modes of 8237 DMA controller.
10.	a)	List the operating modes of 8255A PPI.
	b)	Write a BSR control word subroutine to set bits PC5 and PC7 and reset them after 15 millisecond. Assume that delay subroutine is available.
	c)	In Mode 1 operation of 8255 PPI, what are the control signals when ports A and B act as input ports? Discuss the control signals
	d)	Describe the priority scheme and EOI scheme of 8259.
		5

CS/B.TECH/CSE(O)/ODD/SEM-5/CS-502/2019-20

11. a)	Explain the operations of BIU and EU pres 8086 microprocessor.	sent in
b)	What is the difference between MAX operation and MIN Mode operation in microprocessor?	
c)	How is pipelining achieved in microprocessor?	8086
d)	Explain how 20 hit physical address is general 8086 microprocessor?	ited in