

8085 & 8086 mp MCQ Quiz

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The content of "HL" register pair is 204Ah. What will be the content of "HL" register pair after executing the instruction DAD H. 1 point

- 204Ah
- 4098h
- 4094h
- 2096h

To initiate DMA data transfer the signal to be sent to the CPU is 1 point

- READY
- INTR
- HOLD
- None of these



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READY signal in 8085 is useful when the CPU communicates with

1 point

- slow peripheral device
- A fast peripheral device
- A DMA controller chip
- A PPI chip

Which interrupt has the highest priority?

1 point

- INTR
- TRAP
- RST6.5
- RST7.5

In 8085 name the 16 bit registers?

1 point

- Stack pointer
- Program counter
- A & B
- None of these

In an 8085, after the execution of XRA A instruction

1 point

- The carry flag is set
- The accumulator contains FFH
- The content of accumulator is shifted by one
- The zero flag is set



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The number of flags of the 8085 microprocessor is

1 point

- 6
- 5
- 4
- 3

Why 8085 processor is called an 8 bit processor?

1 point

- Because 8085 processor has 8 bit ALU.
- Because 8085 processor has 8 bit data bus.
- A & B.
- None of these.

Which stack is used in 8085?

1 point

- FIFO
- LIFO
- FILO
- LILO

Accumulator is

1 point

- Counter
- Register
- Keyboard
- None



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The contents of Program Counter (PC), when the processor is reading from 2FFF H location, will be 1 point

- 2FFE H
- 2FFF H
- 3000 H
- 3001 H

In 8085A microprocessor ALE signals made high to 1 point

- Enable the data bus to be used as low order address bus
- To latch data D0-D7 from data bus
- To disable data bus
- To achieve all the functions listed above

What does microprocessor speed depends on? 1 point

- Clock
- Data bus width
- Address bus width
- None



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The number of register pairs of 8085 microprocessor are

1 point

- 3
- 4
- 2
- 5

PSW in the 8085 microprocessor is a

1 point

- 8-bit register
- 16-bit register
- 4-bit register
- 32-bit register

The address lines required for 16K byte memory chip are

1 point

- 13
- 14
- 15
- 16

In 8085 the addressable memory is

1 point

- 64kB
- 1MB
- 4kB
- 16kB



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SP (stack pointer) register holds the

1 point

- Base address of stack
- Address of stack top
- Address of the instruction to be fetched
- None of these

MOV A, M is executed by

1 point

- 1 machine cycle
- 3 machine cycle
- 4 machine cycle
- 2 machine cycle

When PUSH instruction is executed, the stack pointer register is

1 point

- decremented by two
- incremented by two
- decremented by one
- incremented by one

The program counter(PC) in a microprocessor

1 point

- keeps the address of the next instruction to be fetched
- counts the number of instructions being executed on the microprocessor
- count the number of program being executed on the microprocessor
- counts the number of interrupts handled by the microprocessor



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The BSR mode in 8255 is used with one of the following

1 point

- port A
- port B
- port C
- none of these

what are the conditions that BIU can suspend fetching instruction?

1 point

- current instruction requires access to memory or I/O port
- a transfer control (jump or call) instruction occurs
- transfer queue is full
- none of these

Machine cycles in "CALL" instruction are

1 point

- 6
- 5
- 4
- 3

PSW(program status word) is a -----register

1 point

- 8 bits
- 16 bits
- 20 bits
- 32 bits



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The call location for TRAP interrupt is

1 point

- 0000 h
- 0020h
- 0024h
- 0034h

In DMA operation, data transfer takes place between

1 point

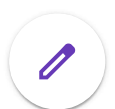
- Memory and CPU
- CPU and I/O
- I/O and Memory
- different CPUs

When a subroutine is called, the address of the instruction next to "CALL" is saved in

1 point

- stack pointer register
- program counter
- stack
- PSW

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the vector address corresponding to software interrupt RST7 in 8085 is

1 point

- 0017h
- 0027h
- 0038h
- 0700h

The CWR address of 8255 PPI connected to 8085 is FBh, what will be the address for Port-A?

1 point

- F8h
- FAh
- FCh
- F9h

OUT 02 H is executed by

1 point

- one machine cycle
- two machine cycle
- three machine cycle
- four machine cycle



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If a DMA request is sent to the microprocessor with a high signal to the HOLD pin, the microprocessor acknowledges the request 1 point

- after completing the present cycle
- immediately after receiving the signal
- after completing the program
- none of these

The stack and stack pointer

1 point

- both reside in memory
- both reside in CPU
- former reside in memory and the later in CPU
- none of these

The addressing mode of the instruction LDAX B is

1 point

- direct
- register indirect
- implicit
- immediate



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The instruction PCHL

1 point

- stores the content of HL pair to a specified memory location
- copies the content of HL pair to the program counter
- stores the content of HL pair to accumulator
- exchanges the content of HL pair with the program counter

Which of the following signals indicates an 8-data transfer from odd address bank? 1 point

- A0=0 and BHE=0
- A0=1 and BHE=1
- A0=0 and BHE=1
- A0=1 and BHE=0

A single instruction to clear the higher four bits of the accumulator in 8085 microprocessor is 1 point

- XRI 0FH
- ANI F0H
- ANI 0FH
- XRI F0H



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Which one of the following is not a NON-Maskable interrupt of 8085 microprocessor?

1 point

- TRAP
- INTR
- RST 7.5
- RST 3

Length of physical address in 8086 is

1 point

- 16 bit
- 4 bit
- 24 bit
- 20 bit

The 8051 microcontroller has

1 point

- 128 bytes on chip RAM
- 8 K bytes on chip ROM
- 16 K bytes on chip RAM
- 32 K bytes on chip ROM

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