Peripheral Interface IC 8255

Microprocessor and Micro-Controller

Course Material – EC 403

- Functional description of Pins
- Programming the PPI
- Modes of Operation
- Interfacing with 8085

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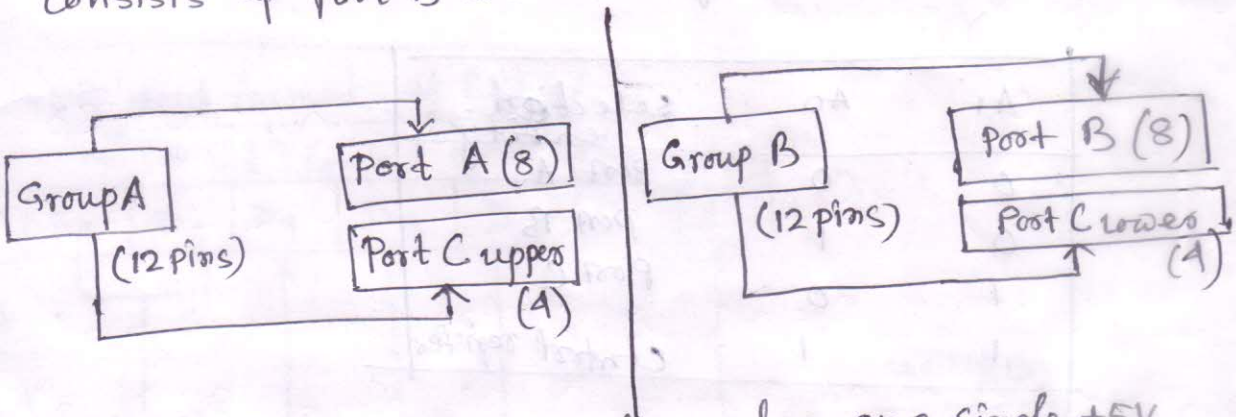
(1) 8255 - Programmable Peripheral Interface (PPI)

Intel has designed an IC, the 8255, with the objective of interfacing input and output devices with Intel microprocessors.

8255 is a programmable peripheral interface IC and is a multi-port input/output device. There are 24 I/O pins, which may be individually programmed in 2 groups of 12 and used, in 3 major modes of operation. The two groups of 12 I/O lines are called Group A and Group B.

Each group contains a subgroup of eight-bit port and a subgroup of four-bit port.

This IC has three eight-bit ports: Port A (PA_7-PA_0) Port B (PB_7-PB_0) and Port C (PC_7-PC_0). The Port C is divided into subgroups such as Port C upper (PC_7-PC_4), and Port C lower (PC_3-PC_0). Group A consists of Port A and Port C upper. Group B consists of Port B and Port C lower.



* 8255 is a 40-pin IC package and operates on a single +5V dc supply.

Functional description of pins

1) Port A (8-bit I/O pins)
2) Port B (8-bit I/O pins)
3) Port C (8-bit I/O pins)
4) D_7-D_0 (Bidirectional 8-bit databus)
5) $\overline{CS}$ (chip select pin which is active low)
*9) V_{cc} (+5V dc) & GND.
(6) $\overline{RD}$ (Read) & $\overline{WR}$ (write) Control signals
(7) RESET
(8) A_0 - A_1 → are normally connected to the least significant bits of the address bus A_0 and A_1. * and are used to select ports and control word register (CWR)

has been 'interfaced' to three I/O devices using the 8255 as a temporary storage space. Thus, the 8255 has three sets of '8-bit parallel ports', which act as intermediary between a processor and a number of I/O devices. Note that in all cases the I/O devices used have only 8-bit data capability – so, only the lower data lines D0-D7 are connected to the 8255.

However, it is a 'programmable chip' as are all the chips we will learn in the next two chapters as well. Keep in mind that these 'interfacing chips' do not have any 'processing' capability. They can only be made to act in the way we want to by 'programming' it using the instructions of 8086 (i.e., the processor to which it is connected). However, they have the hardware to do the special functions that are needed for each specific purpose. Programming interfacing chips entails writing of 'control words' in their control/command registers. We will learn this idea, starting with the 8255.

9.2.1 | Pin Configuration and Internal Block Diagram

Figure 9.3 shows the pin configuration of the DIP (dual-in-line) version of the chip. We see that it has 40 pins, which consist of three 8-bit ports named Port A (PA), Port B (PB) and Port C (PC), each of which can be programmed as input or output ports. Figure 9.4 shows the internal block diagram of the chip. It is seen to consist of various functional blocks, and let us take a quick look at each of the blocks.

Data Bus Buffer There is a three state bi-directional 8-bit buffer which is used to interface the chip to the data bus of the system. Upon execution of the processor's input or output instructions, data and control/status words are received or transmitted by the buffer.

Read/Write Control Logic It manages all data transfer between the chip and the processor on accepting control signals from the control and address buses of the system.

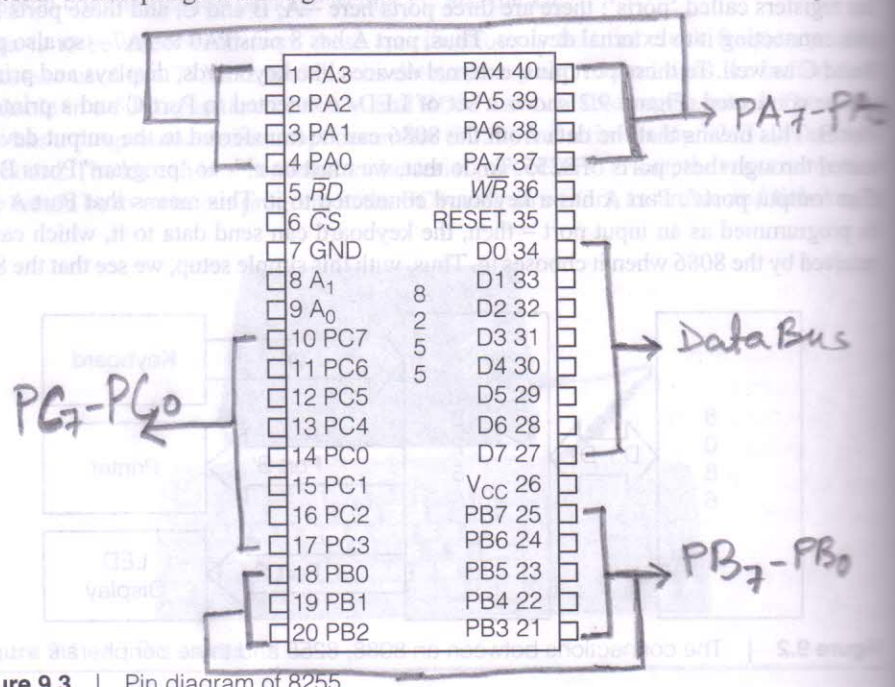


Figure 9.3 | Pin diagram of 8255

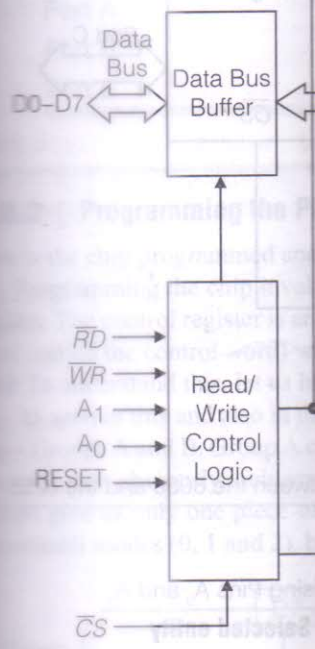


Figure 9.4 | Internal block di

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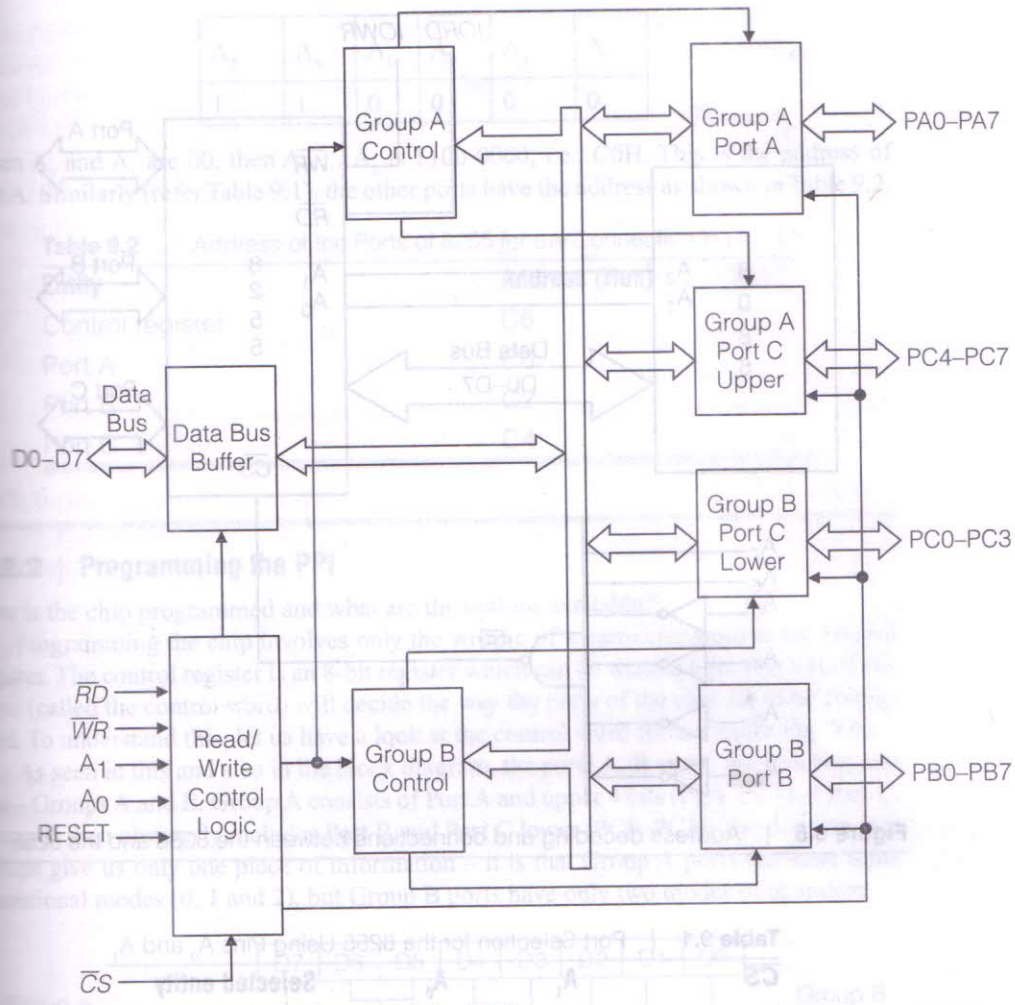
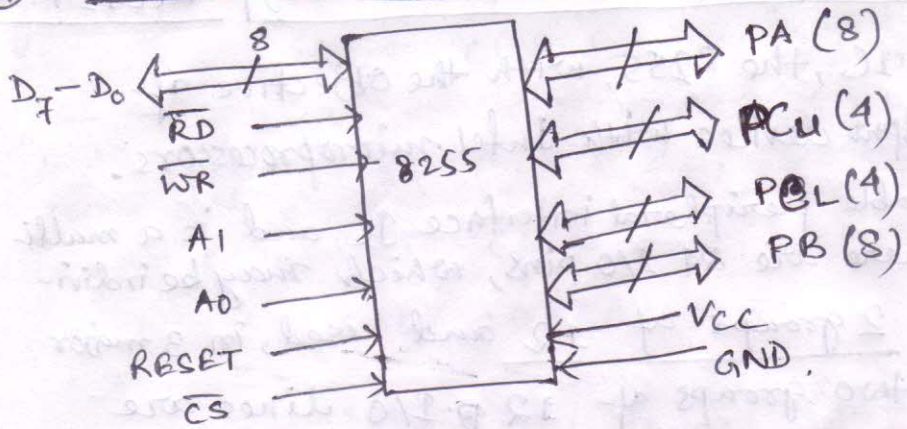


Figure 9.4 | Internal block diagram of the 8255

Group A and B Controls Functionally, this chip has been divided as Group A and B and they have their corresponding controls. We will soon see what this grouping is intended for. The way the chip is to act is decided by a register called the control/status register, which can be written to and read from. Now see a typical connection between the 8086 and an 8255 in Fig. 9.5. The lower data lines of the chip can be connected to 8 bits of the data bus of the 8086. The $\overline{RD}$ and $\overline{WR}$ are connected to the $\overline{IORD}$ and $\overline{IOWR}$ generated from the 8086. If this chip (which is viewed as an I/O port by the processor) is to have only an eight-bit address, only the lower 8 lines of the address lines of the processor need to be involved in the address decoding process, which causes the $\overline{CS}$ line to be activated. Otherwise, 16 address lines may be used. (Recollect that no I/O port can have an address size greater than 16 bits.) Any two address pins of the processor are to be connected to the pins A_0 and A_1 of the 8255.This is because there are four separate entities associated with this chip, and each one needs a unique address. This is achieved by the four possible combinations of these two lines, as shown in Table 9.1.

④ Schematic pin diagram of 8255:



If we see the internal structure of the IC, we will find that, in addition with the three 8-bit I/O ports, there is another register called control register or control word register (CWR).

To identify the 3 ports and control register, the 8255 uses two address lines – A0 and A1. These lines get their signals from the 8085 processor address bus. The identification of the ports and register ~~are~~ based on A0 and A1. is given in Table:

A1	A0	selected entity
0	0	Port A
0	1	Port B
1	0	Port C
1	1	control register.

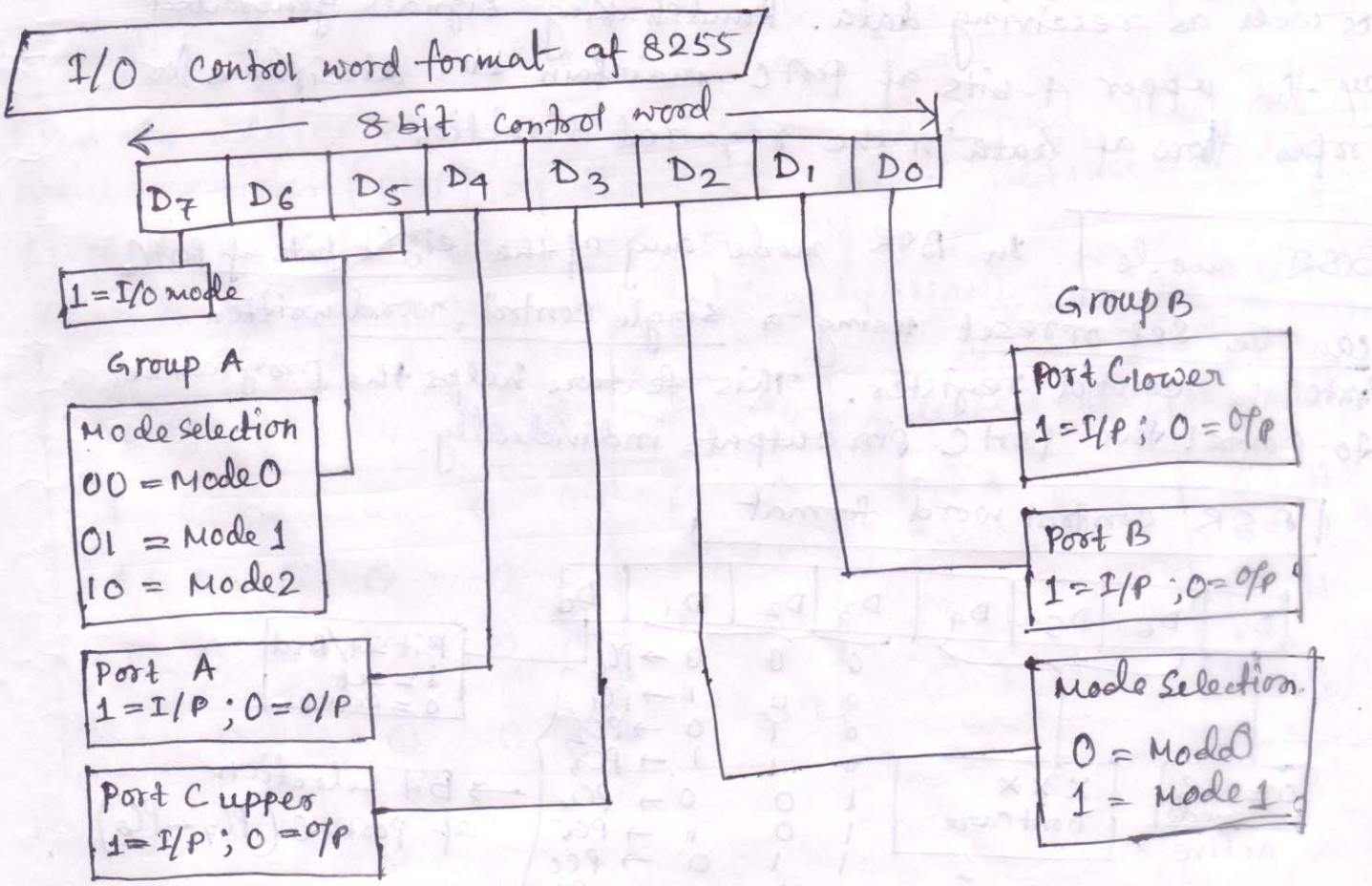
Programming the PPI programming the chip involves only the writing of a particular word to the control register. The control register is an 8-bit register which can be written into. The bits of this word (called the control word) will decide the way the ports of the chip are to be configured. To understand this, let us have a look at the control word format.

Bit Assignment of the Control word.

First, look at D7 bit → it suggests the options of I/O mode or BSR (bit set reset) mode. I/O mode is the normal mode of operation and BSR is a special mode catering to port C alone.

Operating modes.

- I/O mode (D7 bit = 1)
  - → Mode 0 — Basic I/O (Applicable to ports A, B and C)
  - → Mode 1 — Handshake I/O (Applicable to groups A and B)
  - → Mode 2 — Bidirectional I/O. (applicable to group A only)
- BSR mode (D7 bit = 0).



Modes of Operation

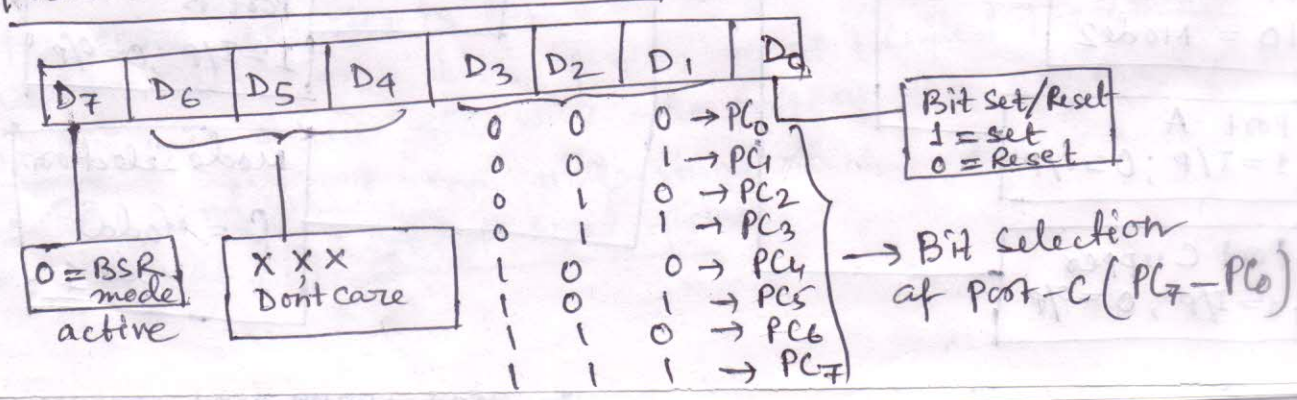
Mode 0 :- This is the simplest and most widely used mode. In this mode, the two 8-bit ports A and B and the 4-bit ports port C upper and port C lower may be used independently. Here, data is simply taken in from an I/P port or given to an o/p port.

Mode 1 :- This is the 'handshaking' mode. Handshake implies data transfer in which the communicating devices exchange request and acknowledge control signals with each other. For an 8255 operating in this mode, ports A and B pins are used for data transfer, while 4 bits of each of port C are used for generating the handshaking signals for each of the 8-bit ports.

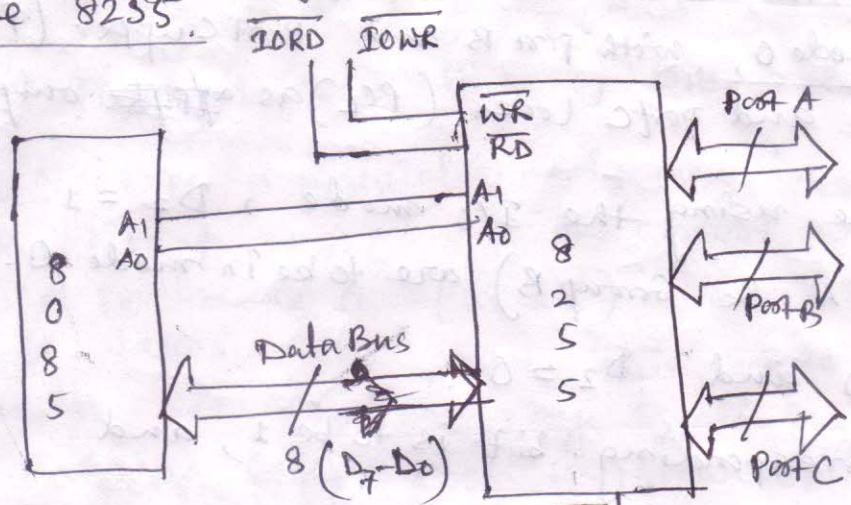
Mode 2 :- This is the bidirectional mode. Only Group A can use this mode. Here, Port A is used for transmitting as well as receiving data. Handshaking signals generated by the upper 4-bits of port C maintain bus discipline for proper flow of data in the required direction.

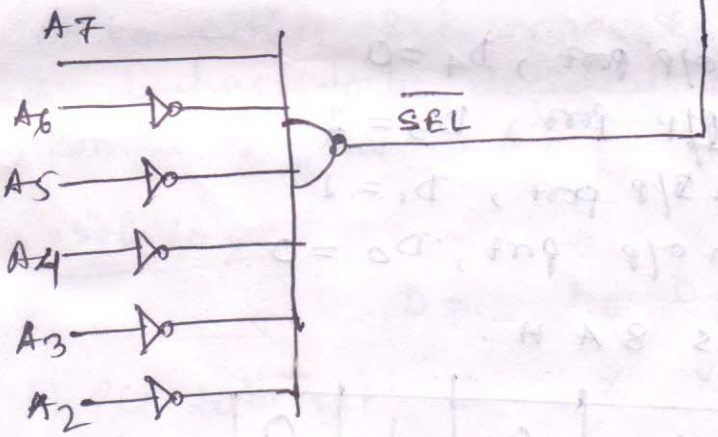
BSR mode In BSR mode, any of the eight bits of port C can be set or reset using a single control word written into the control register. This feature helps the programmer to control the port C pin outputs individually.

BSR control word format



* Address decoding and connections between the 8085 and the 8255.





CS	A1	A0	Selected entity
0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	CWR

Example 1 :-

Find the addresses of Port A, Port B, Port C and the control word register (CWR) of the 8255 whose address decoding circuitry is given in the above figure.

* (When the chip gets selected/enabled NAND gate op should be 0 $\overline{CS} = 0$)

A7	A6	A5	A4	A3	A2	A1	A0	Selected entity	Port Address
1	0	0	0	0	0	0	0	Port A	80 H
1	0	0	0	0	0	0	1	Port B	81 H
1	0	0	0	0	0	1	0	Port C	82 H
1	0	0	0	0	0	1	1	CWR	83 H

Example 12 Design the control word to configure the ports of an 8255 chip in mode 0, with port B and port C upper (PC_U) as inputs and port A and port C lower (PC_L) as ~~inputs~~ outputs.

Ans. Since we are using the I/O mode, $D_7 = 1$

Both groups (Group A & Group B) are to be in mode 0.

Hence, $D_6 D_5 = 00$ and $D_2 = 0$.

For input, the corresponding bit is to be 1, and

for output, it is to be 0.

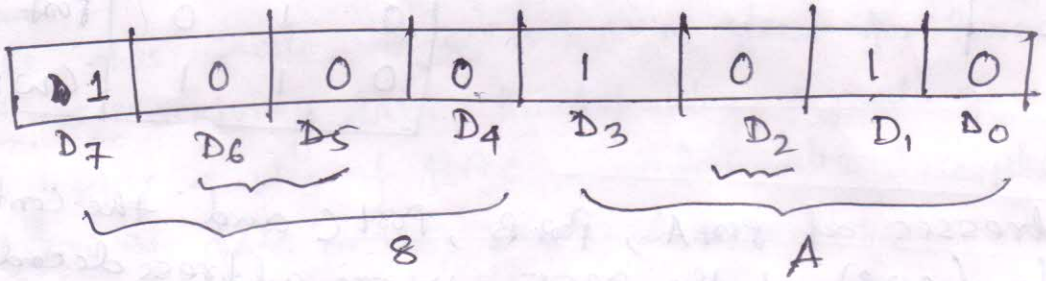
Since Port A is to be an o/p port, $D_4 = 0$

Since Port C_U is to be an I/P port, $D_3 = 1$.

Since Port B is to be and I/P port, $D_1 = 1$

Since Port C_L is to be an o/p port, $D_0 = 0$.

Thus the control word is 8A H.



Imp: The following program instructions will configure the control word of the 8255.

```
MVI A, 8A H   ; Load the control word in the Accumulator.
OUT 83 H      ; Transfer it to the control register of the
                8255. ( 83H is the port address
                of the control word register.)
```

* So the program for initializing the 8255 and outputting data available in Port B to Port A is given below:

```
MVI A, 8A H
OUT 83 H
IN  81 H ; Get data from Port B to the accumulator
OUT 80 H ; Move it to Port A.
```

Example :3 write the BSR control words for the following cases :

(i) PC_0 to be set (ii) PC_7 to be reset (iii) PC_1 to be set (iv) PC_7 to be set

Ans [This is a special mode and is applicable only for the bits of PortC. In the control word format, if the MSB is made 0 ($D_7 = 0$), the BSR (bit set/reset) mode takes effect. In this mode, any bit of PortC can be set or reset by specifying the bit which has to be set or reset. However, at a time, only one bit can be addressed – and that bit is to be either set or reset. The corresponding control word has to be decided and moved to the control register (CWR).]

Solution :-

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
i) PC_0 to be set:	0	X	X	X	0	0	0	1	= 01 H

Considering 'X' cares as '0'.

ii) PC_7 to be reset:	0	0	0	0	1	1	1	0	= 0E H
iii) PC_1 to be set :	0	0	0	0	0	0	1	1	= 03 H.
iv) PC_7 to be set :	0	0	0	0	1	1	1	1	= 0F H]

* Here $D_0 = 1$ means Set ; & $D_0 = 0$ means reset.

* In the BSR mode PORT C should be in O/P mode.

Imp Q:- Generate a square pulse having 50% duty cycle in BSR mode using PC_7 pin.

Steps: 1) write a delay Subroutine using Reg. Pair.
2) Configure the 8255 in mode 0, considering all the ports as in o/p mode [control word will be 80 H]
3) Then write the control word to Set PC_7 pin & to reset PC_7 pin.

Main Program :-

```
        MVI  A, 80H.   ; Load control word into accumulator
        OUT  CWR       ; to configure 8255 in mode0.
                       ; and all ports are in o/p mode.
Loop:   MVI  A, 0FH    ; Control word to set the
                       ; PC7 pin.
        OUT  CWR
        CALL DELAY
        MVI  A, 0E     ; control word to reset the
                       ; PC7 Pin.
        OUT  CWR       ; [CWR Give & PortAdd ;]
        CALL DELAY
        JMP  Loop
```

Subroutine prog:

Delay prog. using Reg. Pair.

Remarks :- You will get a square pulse at point PC7.

50% duty cycle means, ON and OFF time of the pulse will be of equal width.