8085 Interrupts

Microprocessor and Micro-Controller

Course Material – EC 403

By

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Interrupt is a mechanism by which the processor (CPU) is made to transfer Control from its current program execution to another program of more importance or higher priority.

In general, interrupts are generated by a variety of Sources, either internal or external, to the CPU. I/P and O/P devices obtain the service of the CPU by using the interrupt process.

ISR (Interrupt service routine) :- The program or the routine that is executed upon interrupt is called interrupt service routine (ISR).

After execution of the ISR, the processor must return to the interrupted program.

IVA (The address of the memory, where the ISR is located for a particular interrupt signal, is called interrupt Vector address (IVA).

Types of Interrupts

Interrupts are classified based on their maskability, interrupt vector address, and Source.

Classification based on
● Maskability → Maskable Interrupts (RST 7.5, RST 6.5, RST 5.5)
→ Non-maskable Interrupts (TRAP)

The 8085 μp includes four maskable interrupts and one nonmaskable interrupt. The microprocessor can ignore or delay a maskable interrupt request if it is performing some critical task. However it has to respond to a non-maskable interrupt request immediately.

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Classification -

- Based on interrupt vector address → vectorred interrupts (TRAP, RST7.5, RST6.5, RST5.5)
  → non-vectored Interrupts (INTR)

Vectored interrupts have fixed interrupt vector address for ISRs whereas for non-vectorred interrupts require external H/W to supply a call location to restart the execution.

Interrupt	Interrupt Vectoraddress	Maskable or non-maskable
TRAP	0024 H	Non-maskable
RST7.5	003C H	Maskable
RST6.5	0034 H	Maskable
RST5.5	002C H	Maskable
INTR	Decided by External H/W	Maskable.

*Among these five interrupts only RST 7.5 interrupt is edge-triggered and other four are level-triggered.

- Classification Based on their source → Software interrupts (RST0 → RST7)
  → Hardware interrupts. (TRAP, RST7.5, RST6.5, RST5.5, INTR)

✓ software interrupts are Special instructions, which after execution transfer the control to a predefined ISR. These instructions are included in the program by the programmer. Ex: for. RST1, CALL Locationis 0008H.

✓ H/w interrupts are signals given to the processor, for recognition as an interrupt and execution of the corresponding ISR. There are five signal pins in 8085 up.

Questions

* 7) w.a.p. to enable all the interrupts in 8085 after rece

* 6) Explain the function of instructions (a) EI (b) DI (c) SIM (d) RIM.

1) Q. Explain the interrupt process in 8085 up.

Ans. (R. Gaonkar Pg - 377)

2.) Q. Define the following terms. (a) ISR (b) IVA (c) H/w interrupt (d) S/w interrupt (e) Vectored interrupt (f) Non-vectored interrupt (g) Maskable interrupt (h) Non-maskable interrupt.

Ans. (Note).

3) Q. What is meant by priority of interrupt ?

– Interrupt priority decides which interrupt must be serviced when more than one interrupt is sensed by the processor.

Priority.	Interrupt
1	TRAP (Highest priority)
2.	RST 7.5
3.	RST 6.5
4.	RST 5.5
5.	INTR (Lowest priority)

4). What is the location of ISR for RST 5.5 interrupt.

$(5.5 \times 8) = 44_{10}$ $(44)_{10} \rightarrow (2C)_H$

∴ CALL location → 002CH.

5) The concept of priority doesnot apply to S/w interrupts. Why ?

Ans. As they are inserted into the program as instructions by the programmer and executed by the processor when the respective program lines are read.

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* 5.11 MASKING OF INTERRUPTS

Masking can be done for the four hardware interrupts RST 7.5, RST 6.5, RST 5.5, and INTR. The masking of 8085 interrupts is done at different levels. Figure 5.8 shows the organization of hardware interrupts in the 8085. The figure clearly shows that TRAP is an NMI. RST 7.5 interrupt alone has a flip-flop to recognize its edge transition. The masking of interrupts can be done using SIM instruction. In addition, a separate interrupt enable flip-flop is available to mask or allow the interrupts. Figure 5.8 is explained in detail by the following five points.

(i) The maskable interrupts are, by default, masked by the Reset signal. So no interrupt is recognized by the hardware reset.

(ii) The interrupts can be enabled by the execution of the EI instruction. So to enable the interrupts after resetting the processor, the EI instruction must be used.

(iii) The three RST interrupts can be selectively masked by loading the appropriate word in the accumulator and executing the SIM instruction. This is called *software masking*.

(iv) All the maskable interrupts are disabled whenever an interrupt is recognized. So, it is necessary to execute the EI instruction every time the interrupts are recognized and serviced by the processor.

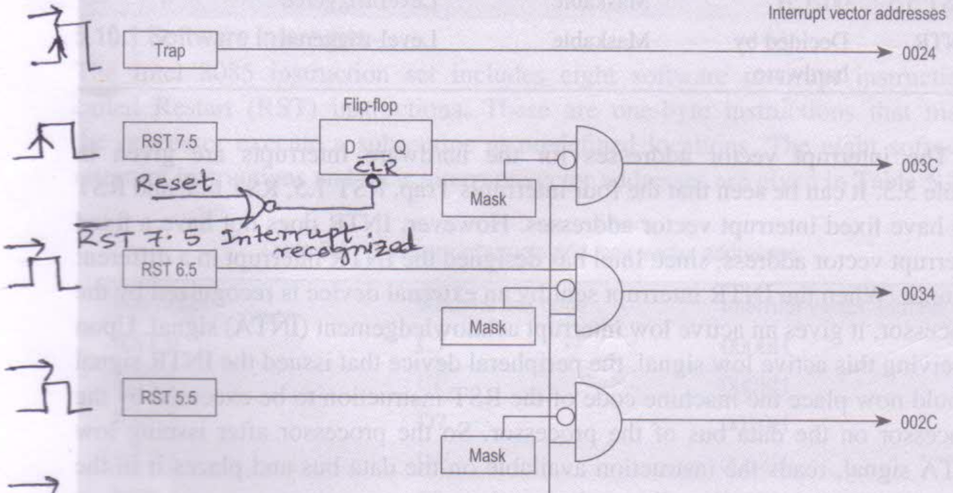

Fig. 5.8 Interrupt structure of Intel 8085

(v) All the maskable interrupts can be disabled by executing the DI instruction. This instruction resets an interrupt enable flip-flop in the processor and the interrupts are disabled. To enable interrupts, EI instruction has to be executed.

5.11.1 SIM Instruction

The SIM instruction is used to mask or unmask the restart (RST) hardware interrupts. The SIM instruction when executed reads the contents of the accumulator and accordingly masks or unmasks the interrupts. So the SIM instruction must be executed after storing the appropriate control word in the accumulator. The format of the control word to be stored in the accumulator before executing the SIM instruction is shown in Table 5.6.

Table 5.6 Accumulator bit pattern for SIM instruction

Bit position	D7	D6	D5	D4	D3	D2	D1	D0
Name	SOD	SDE	X	R7.5	MSE	M7.5	M6.5	M5.5
Explanation	Serial data to be sent	Serial data enable—set to 1 for sending	Not used	Reset RST 7.5 flip-flop	Mask set enable—Set to 1 to mask interrupts	Set to 1 to mask RST 7.5	Set to 1 to mask RST 6.5	Set to 1 to mask RST 5.5

The least significant three bits D2–D0 are used to individually mask the three RST interrupts, as shown in Table 5.6. These bits are made 0 to unmask the interrupts and 1 to mask the interrupts. In addition, a master control is also provided in the D3 bit. This bit must also be set to 1 to make the least significant three bits meaningful. Otherwise, the data in the least significant three bits are ignored by the processor.

As already discussed, the RST 7.5 is an edge-triggered interrupt and a separate flip-flop is used to recognize it. This flip-flop can be reset, thereby ignoring the RST 7.5 interrupt. This is done by making the D4 bit 1.

In addition to masking interrupts, the SIM instruction has another function. It can send serial data on the SOD line of the processor. The data to be sent is placed in the MSB of the accumulator and the serial data output is enabled by making the D6 bit 1.

5.11.2 RIM Instruction

The RIM instruction is used to read the status of the interrupt mask bits. When the RIM instruction is executed, the accumulator is loaded with the current status of the interrupt masks and the pending interrupts. The format and meaning of the data stored in the accumulator after execution of the RIM instruction is shown in Table 5.7.

The least significant three bits of the accumulator after executing RIM instruction indicate whether the RST hardware interrupts are masked. The presence of the bit 1 indicates that the corresponding interrupt is masked.

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Table 5.7 Accumulator bit pattern after execution of RIM instruction

Bit position	D7	D6	D5	D4	D3	D2	D1	D0
Name	SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5
Explanation	Serial input data in the SID pin	Set to 1 if RST 7.5 is pending	Set to 1 if RST 6.5 is pending	Set to 1 if RST 5.5 is pending	Set to 1 if interrupts are enabled	Set to 1 if RST 7.5 is masked	Set to 1 if RST 6.5 is masked	Set to 1 if RST 5.5 is masked

All the hardware interrupts can be masked by executing the DI instruction. To check whether the interrupts are enabled or disabled, the programmer can check the D3 bit of the accumulator after executing the RIM instruction. If the D3 bit is set to 1, it means that the interrupts are enabled. The bits D4–D6 indicate whether there are any RST interrupts pending. Logic 1 on these bits indicates that the corresponding interrupts are pending.

In addition to reading the interrupt mask, the RIM instruction is also used to read the serial data on the SID pin of the processor. The data on the SID pin is stored in the MSB of the accumulator after execution of the RIM instruction.

Example:

Write the assembly language program lines to enable all the interrupts in the 8085 after reset.

After reset, all the interrupts are disabled as shown in Fig. 5.8. So, the EI instruction must be executed. To enable all RST interrupts, the corresponding bits in the accumulator pattern must be 0 and the Mask Set Enable bit must be 1 before executing the SIM instruction.

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EI                ; Enable interrupts.
MVI A, 00001000B  ; Unmask the interrupts.
SIM               ; Set the mask and unmask using SIM instruction.
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5.12 TIMING OF INTERRUPTS

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The interrupts are sensed by the processor one cycle before the end of execution of each instruction. An interrupt signal must be applied long enough for it to be recognized. The longest instruction of the 8085 takes 18 clock periods. So, the interrupt signal must be applied for at least 17.5 clock periods. This decides the minimum pulse width for the interrupt signals.

The maximum pulse width for the interrupt signals is decided by the condition that the interrupt signal must not be recognized once again. This is under the control of the programmer. Once an interrupt is recognized, all interrupts are disabled. The re-enabling of interrupts is done by executing the instruction EI. So, the maximum duration for the interrupts is decided by the execution of the EI instruction. The interrupt signal must be removed before the EI instruction is executed so that it will not be recognized once again.